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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,031	09/18/2003	Anthony G. Aipperspach	ROC920030045US1	7942

30206 7590 02/15/2006

IBM CORPORATION
ROCHESTER IP LAW DEPT. 917
3605 HIGHWAY 52 NORTH
ROCHESTER, MN 55901-7829

EXAMINER	
CHASE, SHELLY A	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,031	AIPPERSPACH ET AL.	
	Examiner	Art Unit	
	Shelly A. Chase	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 9-18-2003.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

SHELLY CHASE
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 to 8 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1** to **6** are rejected under 35 U.S.C. 102(b) as being anticipated by Abdoo et al. (USP 5490155).

Claims **1** and **4**:

Abdoo teaches the claimed invention. Abdoo teaches a method and a device for detecting single, two adjacent bit errors and four adjacent bit errors using an error detection and correction system; the device comprising: a memory array (32) coupled to system data buffer (44 & 45) for storing data word and associated check bits (see col. 3, lines 4 to 6 and col. 4, lines 3 to 7). Abdoo teaches that during a read cycle data bits and check bits are outputted for error correction and detection (see col. 5, lines 32 to 40) and upon the receipt of a check bit enable signal (CHK_EN) from computer C an error detection is performed for the read data bits (see col. 8, lines 30 et seq.), interpreted as "activating each of a line of a memory boundary in a memory array having the parity bit."

Abdoo also teaches that two identically check bit generators ("parity checking devices") receive alternating pairs of data to detect two adjacent bit errors (see col. 6, lines 40 et seq.). Abdoo teaches that bits (0, 1) are directed to the first check bit generator and bits (2, 3) are directed to the second check bit generator (see col. 3, lines 1 to 5 and col. 9, lines 35 et seq.). Abdoo further teaches that a two bit errors can be detected using the b-adjacent error correction code taught by Bossen (see col. 7, lines 24 et seq.).

As per claims **2** and **5**, Abdoo teaches that an error detection and correction circuit (82) detects and corrects errors of adjacent bit pairs (see col. 8, lines 31 et seq.).

As per claims **3** and **6**, Abdoo teaches that two identical check bit generators receive alternating pair of bits for the detection of two adjacent bit errors and four adjacent bit errors (see col. 7, line 10 to 20).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims **7** to **8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Abdoo et al. (USP 5490155) in view of Nakamura et al. (*Giga-bit DRAM cells with low*

capacitance and low resistance bit-lines on buried MOSFET's and capacitors by using bonded SOI technology-reversed-stacked-capacitor (RSTC) cell, IEEE).

As per claims **7** and **8**, Abdoo does not specifically teach that the memory array is constructed on a silicon on insulator (SOI) metal oxide semiconductor (MOS) or on bulk silicon; however, Nakamura in an analogous art teaches that a conventional dynamic random access memory (DRAM) comprises metal oxide semiconductor field effect transistors (MOSFET) wherein bulk MOSFET's are turned to SOI-MOSFET's using a bonded-SOI process (see pg. 35.4.1). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the DRAM cells of the memory array of Abdoo to include DRAM cells comprising SOI-MOSFET technology since, Nakamura teaches that the use of SOI bonding technology improves soft error immunity. This modification would have been obvious because a person of ordinary skill in the art would have been motivated to employ a DRAM cell for its advantages of reducing errors as taught by Nakamura.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelly A. Chase whose telephone number is 571-272-3816. The examiner can normally be reached on Mon-Thur from 8:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SHELLY CHASE
PRIMARY EXAMINER